UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/648,743	08/26/2003	Robert M. Grow	P8850C	3732

50890 7590 10/15/2007

CAVEN & AGHEVLI
c/o INTELLEVATE
P.O. BOX 52050
MINNEAPOLIS, MN 55402

EXAMINER	
WILSON, ROBERT W	

ART UNIT	PAPER NUMBER
2619	

MAIL DATE	DELIVERY MODE
10/15/2007	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/648,743	GROW, ROBERT M.	
	Examiner	Art Unit	
	Robert W. Wilson	2619	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *13 August 2007*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1,7,13 and 19-29* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1, 7, 13, & 19-29* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

Claim Rejections - 35 USC § 103

1. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

2. Claims 1, 7, 13, & 28-29 are rejected under 35 U.S.C. 103(a) as being unpatentable over Ferguson (U.S. Patent No.: 5,809,024) in view of Jugel (U.S. Patent No.: 5,390,174) .

Referring to claim1, Fergurson teaches: a method of transmitting data frame to a plurality of output ports, each of the data frame having a destination associated with one of the output ports (Hub per Fig 2 performs the method) , the method comprising:

at each of a plurality of input ports, portioning a portion of each data frame to provide one or more order data cells having data representative of a sequence number corresponding with the output port associated with the destination of the data frame the data representative of the sequence number in each data cell indicating an ordinal position of the data cell among the ordered data cell of the data frame (Each LAN nodule has a plurality of input ports (211B) which segments or partitions a data packet or data frame into one or more ATM or data cells corresponding to an output port (241A) associated with the destination of the data packet or data frame per Fig 2 and per col. 8 line 34 to col. 9 line 67); and

at each of the output port, receiving a forwarded data cell for each order data cell associated with each data frame having a destination associated with the output port, each forwarded data cell corresponding with an ordered data cell and data frame associated with the ordered data cell and determining an ordinal position of the forwarded data cell among the forwarded data cell associated with the data frame based upon data in the forwarded data cell representative of the sequence number (Each of the output ports (LAN Module 204 has a plurality of output ports 241A) which receive the forwarded ATM cells associated with the segmented or partitioned data packet or data frame having a destination address associated with output port (241A)

Ferguson does not expressly call for: adding a sequence number representative of the ordinal position and determining the ordinal position of the received cells at the output port but teaches reassembly of the ATM cells into the segmented data packet per col. 8 line 34 to col. 9 line 67

Jugel teaches: adding a sequence number representative of the ordinal position and determining the ordinal position of the received frames at the output port (SEQ or sequence number is added

to the cell which is used by the Resequencer to determine the ordinal position of the received frames per fig 3)

It would have been obvious to one of ordinary skill in the art at the time of the invention to add the sequence number and resequence the received cells of Jugel to the segmented packets prior to reassembly of Ferguson in order to insure that cells are put back into the correct order prior to reassembly.

Referring to claim 7, Ferguson teaches: a data switch (Hub per Fig 2) comprising:

a plurality of output port for transmitting forwarded data forwarded to destinations (LAN Module 201 has a plurality of output ports such as 241A for forwarding the data to Device 224 or destination per Fig 2);

a plurality of input ports for receiving data frame each received data frame having a destination associated with one of the output ports each of the plurality of input ports including logic for partitioning a portion of each received data frame to provide one or more ordered data cells a having the data representative of a sequence number corresponding with the output port associated with the destination of the received data frame, the data representative of the sequence number in each order data cell indicating an ordinal position of the ordered data cell among the order data cell of the frame (LAN module 201 has a plurality input ports for receiving a data packet or frame having a destination for device 224 which is associated with output port 241A . The input port 211B has inherent segmentation logic for segmenting or partitioning the received data packet or data frame into one or more ATM or data cells which correspond with the output port 241A associated with device 224 or destination of the data packet or received frame per Fig 2 and per col. 8 line 34 to col. 9 line 67);

wherein each of the output port receives forwarded data cells, each forwarded data cell corresponding with an ordered data cell generated at one of the input ports and having data indicative of the sequence number of the corresponding ordered data cell and includes logic for determining an ordinal position of the forwarded data cell among the forwarded data cells of the forwarded data frame based upon the data indicative of the sequence number in the forwarded data cell Each of the output ports (LAN Module 204 has a plurality of output ports 241A) which receive the forwarded ATM cells associated with the segmented or partitioned data packet or data frame having a destination address associated with output port (241A)

Ferguson does not expressly call for: adding a sequence number representative of the ordinal position and determining the ordinal position of the received cells at the output port but teaches reassembly of the ATM cells into the segmented data packet per col. 8 line 34 to col. 9 line 67

Jugel teaches: adding a sequence number representative of the ordinal position and determining the ordinal position of the received frames at the output port (SEQ or sequence number is added to the cell which is used by the Resequencer to determine the ordinal position of the received frames per fig 3)

It would have been obvious to one of ordinary skill in the art at the time of the invention to add the sequence number and resequence the received cells of Jugel to the segmented packets prior to reassembly of Ferguson in order to insure that cells are put back into the correct order prior to reassembly.

In addition Ferguson teaches:
Regarding claim 28, wherein application specific integrate circuit (ASIC) buffers receive the forwarded data cells at least of the output ports (inherent buffers receive the segmented packet for reassembly and the reference teaches that applicant invention can be implemented as an integrate circuit or set of chips or ASIC per col. 8 lines 34 to 50)

Referring to claim 13, Ferguson teaches: In a data communication network (LAN segment per Fig 2) including a plurality of host computer (inherent plurality of Devices; such as, 221 per Fig 2) for transmitting data packets (Data packets) to a plurality of network device (plurality of inherent network devices such as 224 per Fig 20 each of the data packet (data packet) having data representative of a destination network address (LAN packet has an inherent destination address) , each of the network device having a media access control (MAC) address associated therewith (Each of the devices 224 per Fig 2 have an inherent MAC address because they are LAN devices)

a plurality of output ports, each of the output ports being coupled to at least an associated one of the network device for transmitting MAC data frame to the at least one network device according the MAC address associated therewith (LAN module 204 per Fig 2 has a plurality of output ports such as 241A which are coupled to device 224 and 241A transmits LAN or MAC data frame to 224 or network device according to an inherent MAC address per col. 8 line 34 to col. 9 line 67)

A loop-up engine for receiving the data packet from the host computers addressed to one or more of the network devices and forming intermediate data frame based upon the data packets, the intermediate data frame having a data payload and information identifying an output port associated with the one or more network devices (LAN Module 201 receives the data packet from the Device (221) or host computer which is addressed to device (224) or network device and the data packet has an inherent payload per Fig 2 and per col. 8 line 34 to col. 9 line 67)

A plurality of input ports for receiving intermediate data frames from the look up engine each received data frame having a destination associated with one of the output ports each of the plurality of input ports including logic for partitioning the data payload of each received intermediate data frame to provide one or more ordered data cells having data representative of a sequence number corresponding with the output port associated with the destination of the received intermediate data frame the data representative of the sequence number in each order data cell indicating an ordinal position of the ordered data cell among the ordered data cells of the intermediate data frame (The LAN Module 201 has a plurality of input ports 211B which receive the data frame from the LAN module or lookup engine each of the received LAN or data

frames has a destination associated with one of the output ports 241A per Fig 2 . Each of the ports 211B have inherent segmentation logic for segmenting or partitioning the data frame of the received data frame into one or more ATM cells associated with the destination for device 224 per Fig 2 and per col. 8 line 34 to col. 9 line 67)

Wherein each of the output ports received forwarded data cells, each forwarded data cell corresponding with an ordered data cell originating at one of the input ports and having data indicative of the sequence number of the corresponding ordered data cell, and includes logic for determining an ordinal position of the forwarded data cell among the forwarded data cell among the forwarded data cell of the forwarded data frame based upon the data indicative of the sequence number in the forwarded data frame based upon the data indicative of the sequence number in the forwarded data cell (LAN Module 204 has a plurality of output ports 241A) which receive the forwarded ATM cells associated with the segmented or partitioned data packet or data frame having a destination address associated with output port (241A) per Fig 2 and per col. 8 line 34 to col. 9 line 67

Ferguson does not expressly call for: lookup engine that creates an intermediate data packet with information identifying the an output port or adding a sequence number representative of the ordinal position and determining the ordinal position of the received cells at the output port but teaches reassembly of the ATM cells into the segmented data packet per col. 8 line 34 to col. 9 line 67

Jugel teaches: lookup engine that creates an intermediate data packet with information identifying the an output port (memory or buffer which has table which upon receipt of a packet or cell with a VPI/VCI adds a port number of information identifying an output port per Fig 3) adding a sequence number representative of the ordinal position and determining the ordinal position of the received frames at the output port (SEQ or sequence number is added to the cell which is used by the Resequencer to determine the ordinal position of the received frames per fig 3)

It would have been obvious to one of ordinary skill in the art at the time of the invention to add lookup table and addition of the the sequence number and resequence the received cells of Jugel LAN module of Ferguson in order to insure that cells are put back into the correct order prior to reassembly.

In addition Ferguson teaches:
Regarding claim 29, wherein application specific integrate circuit (ASIC) buffers receive the forwarded data cells at least of the output ports (inherent buffers receive the segmented packet for reassembly and the reference teaches that applicant invention can be implemented as an integrate circuit or set of chips or ASIC per col. 8 lines 34 to 50)

3. Claims 19-26 are rejected under 35 U.S.C. 103(a) as being unpatentable over Ferguson (U.S. Patent No.: 5,809,024) in view of Jugel (U.S. Patent No.: 5,390,174) further in view of Chuissi (U.S. Patent No.: 5,689,500)

Referring to claim 19, the combination of Ferguson and Jugel teach the method of claim 1 and output ports.

The combination of Fergson and Jugel do not expressly call for: logic indicating the availability of buffer space for receipt of additional cells from a crossbar.

Chiussi teaches: logic indicating the availability of buffer space for receipt of additional cells from a crossbar (logic provides backpressure based upon buffer space available for receipt of cells from a crossbar per Fig 11 and per col. 14 lines 7 to 52)

It would have been obvious to add the crossbar and associated backpressure indication of Chiussi in place of the backplane which performs switching of the combination of Fergsuon and Jugel in order improve performance of switching the cells through the switch relative to overflow.

Referring to claim 20, the combination of Ferguson, Jugel, and Chuissi teach the method of claim 19 and output ports.

The combination of Fergsuon and Jugel do not expressly call for: further including each of the output ports signaling to each of a plurality of cross bar sections each of the output ports ability to accept additional data cell in a following cell interval

Chuissi teaches: further including each of the output ports signaling to each of a plurality of cross bar sections each of the output ports ability to accept additional data cell in a following cell interval (backpressure bit map inherently dynamically changes indicting that more cells can be accepted per col. 14 lines 7 to 52)

It would have been obvious to one of ordinary skill in the art at the time of the invention to add the further including each of the output ports signaling to each of a plurality of cross bar sections each of the output ports ability to accept additional data cell in a following cell interval of Chuissi to the system of the combination of Fergsuon, Jugel, and Chuissi in order to build a system which improves the performance relative to overflow.

Referring to claim 21, the combination of Ferguson, Jugel, and Chuissi teach the method of claim 20

The combination of Fergsuon and Jugel do not expressly call: wherein the signals to each of the plurality of crossbar sections occurs via a data bus between each of the output ports and each of the plurality of crossbar sections.

Chuisi teaches: wherein the signals to each of the plurality of crossbar sections occurs via a data bus between each of the output ports and each of the plurality of crossbar sections (signals between stages run on a bus per Fig 14 and per col. 14 lines 7 to 52)

It would have been obvious to one of ordinary skill in the art at the time of the invention to add wherein the signals to each of the plurality of crossbar sections occurs via a data bus between each of the output ports and each of the plurality of crossbar sections Chuissi to the system of the combination of Fergsuon, Jugel, and Chuissi in order to build a system which improves the performance relative to overflow

Referring to claim 22, the combination of Ferguson and Jugel teach the data switch of claim 7 and output ports.

The combination of Fergson and Jugel do not expressly call for: logic indicating the availability of buffer space for receipt of additional cells from a crossbar.

Chiussi teaches: logic indicating the availability of buffer space for receipt of additional cells from a crossbar (logic provides backpressure based upon buffer space available for receipt of cells from a crossbar per Fig 11 and per col. 14 lines 7 to 52)

It would have been obvious to add the crossbar and associated backpressure indication of Chiussi in place of the backplane which performs switching of the combination of Fergsuon and Jugel in order improve performance of switching the cells through the switch relative to overflow.

Referring to claim 23, the combination of Ferguson, Jugel, and Chuissi teach : the data switch of claim 22 and output ports.

The combination of Fergsuon and Jugel do not expressly call for: wherein the logic to indicate the availability of buffer space signals to each of a plurality of crossbar section each of the output ports availability to accept additional data cells in a following cell interface.

Chuissi teaches: wherein the logic to indicate the availability of buffer space signals to each of a plurality of crossbar section each of the output ports availability to accept additional data cells in a following cell interface (backpressure bit map inherently dynamically changes indicting that more cells can be accepted per col. 14 lines 7 to 52)

It would have been obvious to one of ordinary skill in the art at the time of the invention to add wherein the logic to indicate the availability of buffer space signals to each of a plurality of crossbar section each of the output ports availability to accept additional data cells in a following

cell interface of Chuissi to the system of the combination of Ferguson, Jugel, and Chuissi in order to build a system which improves the performance relative to overflow.

Referring to claim 24, the combination of Ferguson, Jugel, and Chuissi teach: the data switch of claim 23

The combination of Ferguson and Jugel do not expressly call: further including a data bus between each of the plurality of the output ports and each of the crossbar section that transfer the signal to indicate the availability of buffer space.

Chuisi teaches: further including a data bus between each of the plurality of the output ports and each of the crossbar section that transfer the signal to indicate the availability of buffer space. (signals (bitmap) runs between stages run on a bus per Fig 14 and per col. 14 lines 7 to 52)

It would have been obvious to one of ordinary skill in the art at the time of the invention to add further including a data bus between each of the plurality of the output ports and each of the crossbar section that transfer the signal to indicate the availability of buffer space of Chuissi to the system of the combination of Ferguson, Jugel, and Chuissi in order to build a system which improves the performance relative to overflow

Referring to claim 25, the combination of Ferguson and Jugel teach: the apparatus of claim 13 and output ports.

The combination of Ferguson and Jugel do not expressly call for: logic indicating the availability of buffer space for receipt of additional cells from a crossbar.

Chiussi teaches: logic indicating the availability of buffer space for receipt of additional cells from a crossbar (logic provides backpressure based upon buffer space available for receipt of cells from a crossbar per Fig 11 and per col. 14 lines 7 to 52)

It would have been obvious to add the crossbar and associated backpressure indication of Chiussi in place of the backplane which performs switching of the combination of Fergsuon and Jugel in order improve performance of switching the cells through the switch relative to overflow.

Referring to claim 26, the combination of Ferguson, Jugel, and Chuissi teach: the apparatus of claim 25.

The combination of Ferguson and Jugel do not expressly call for: wherein the logic to indicate the availability of buffer space signals to each of the plurality of crossbar sections each of the output ports availability to accept additional data cells in the following cell interval

Chuissi teaches: wherein the logic to indicate the availability of buffer space signals to each of the plurality of crossbar sections each of the output ports availability to accept additional data cells in the following cell interval (backpressure bit map inherently dynamically changes indicting that more cells can be accepted per col. 14 lines 7 to 52)

It would have been obvious to one of ordinary skill in the art at the time of the invention to add wherein the logic to indicate the availability of buffer space signals to each of the plurality of crossbar sections each of the output ports availability to accept additional data cells in the following cell interval of Chuissi to the system of the combination of Fergsuon, Jugel, and Chuissi in order to build a system which improves the performance relative to overflow.

Response to Amendment

4. Applicant's arguments with respect to claims 1, 7,13, & 19-29 have been considered but are moot in view of the new ground(s) of rejection.

Conclusion

5. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Robert W. Wilson whose telephone number is 571/272-3075. The examiner can normally be reached on M-F (8:00-4:30).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Edan Orgad can be reached on 571/272-7884. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

Robert W. Wilson
Examiner
Art Unit 2619

RWW
10/11/07